



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

For: CONNECTION METHOD AND
CONNECTION STRUCTURE OF
PAD ELECTRODES, AND
INSPECTING METHODS FOR
CONNECTION STATE THEREOF

Confirmation No.: 7801

Date: October 24, 2002

This preliminary amendment is filed in response to the Office Action dated July 25, 2002 Paper No. 8). Concurrently filed with this preliminary amendment is a Request for Approval of Drawing Changes. Please amend the above-noted application as follows:

Please replace claim 7 as follows.

a substrate having a surface and substrate-side pad electrodes formed on the
 ate surface;

a surface-mount component having a surface, component-side pad electrodes formed on the surface, and a solder bump formed on the component-side pad, the surface being opposed to the substrate with each component-side pad electrode opposed to one of the substrate-side pad electrodes;

wherein the substrate-side pad electrodes are arranged inside a component-
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corresponding region, the length of each of the substrate-side pad electrodes being larger than that of the corresponding component-side pad electrode, and wherein each of the component-side pad electrodes is connected to the corresponding substrate-side pad electrode by a solder which has flowed between the component-side pad electrodes and the substrate-side pad electrodes by melting of the solder bump, and the solder bump is arranged so that a center of the solder bump is located off-set from a center of the substrate-side pad.



REMARKS

This Preliminary Amendment is filed in order to facilitate processing in the above-identified application and is filed in response to the Office Action dated July 25, 2002 in which the Examiner objected to the drawings and rejected claims 7-8 under 35 U.S.C. §103.

Applicants respectfully request the Examiner acknowledge the Information Disclosure Statement filed July 12, 2002.

Concurrently filed with this Preliminary Amendment is a Request for Approval of Drawing Changes in order to correct the drawings and removed the cross hatching. It is respectfully requested that Examiner approves the correction and withdraws the objection to the drawings.

Claim 7 claims a connection structure comprising a substrate and surface-mounted component. The substrate has a surface and substrate-side pad electrodes formed on the substrate surface. The surface-mounted component has a surface, component-side pad electrodes formed on the surface and a solder bump formed on the component-side pad. The surface is opposed to the substrate with each component-side pad electrode opposed to one of the substrate-side pad electrodes. The substrate-side electrodes are arranged inside a component-corresponding region. The length of each of the substrate-side pad electrodes is larger than that of the corresponding component side pad electrodes. Each of the component-side pad electrodes is connected to the corresponding substrate-side pad electrodes by a solder which has flowed between the component-side pad electrodes and the

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substrate-side pad electrode by melting of the solder bump. The solder bump is arranged so that a center of the solder bump is located off-set from a center of the substrate-side pad.

Through the structure of claimed invention having a solder bump arranged so that a center thereof is located off-set from a center of a substrate-side pad, as claimed in claim 7, the claimed invention provides a connection structure which is adaptable to high density mounting. The prior art does not show, teach or suggest the invention as claimed in claim 7.

Claims 7-8 were rejected under 35 U.S.C. § 103 as being unpatentable over *Tanaka* (U.S. Patent No. 5,889,326) in view of *Hiruta* (U.S. Patent No. 5,998,861).

Tanaka appears to disclose a structure for bonding a semiconductor device to a substrate which is provided with: an A1 pad 2 formed on a semiconductor chip 1; a first bump 4 which is composed of a first metal such as Au and which is formed on the pad 2; a plurality of rectangular substrate pads 6 which are arranged on a circuit board 5 at predetermined pitches, and length L of a first side thereof in parallel to the arranging direction is smaller than length M of a second side thereof which is orthogonal to the first side, length L of the first side is smaller than the diameter of the first bump 4, and length M of the second side is larger than the diameter of the first bump 4; and a second bump 7 which is formed on the substrate pad 6, which melts to cover the first bump 4, and which is composed of a second metal such as eutectic Sn/Pb or other metal that is different from the first metal, the width thereof in the direction parallel to the first side being smaller than the diameter of the first bump 4 and the width thereof in the direction parallel to the second side being larger than the diameter of the first bump 4. (col. 3, lines 7-25).

Thus, *Tanaka* merely discloses in Figs. 2-7 solder bumps centered over substrate pads. Nothing in *Tanaka* shows, teaches or suggests that the solder bump is off-set as claimed in claim 7. Rather, *Tanaka* teaches away from the claimed invention since the solder bump is centered over the substrate pad.

Hiruta appears to disclose FIG. 1 shows a conventional semiconductor device having a ball grid array. Ball bumps 2 are formed on a main surface of an LSI (large scale integrated circuit) chip 1. The bumps 2 are formed of metal such as solder. A chip carrier 3 comprises a laminate board 4 having a plurality of layers, wires 5 passing through each layer and each interlayer, electrodes 6a formed on one surface side of the laminate board 4, and electrodes 6b formed on the other surface side of the laminate board 4. The wires 5 electrically connect the electrodes 6a to the electrodes 6b. The electrodes 6b are arrayed on the other surface side of the laminate board 4. Ball electrodes 7 are formed on the electrodes 6b, respectively. The ball electrodes 7 constitute a ball grid array. The ball electrodes 7 are formed of metal such as solder, etc. The LSI chip 1 is combined with the electrodes 6a of one side of the laminate board 4 by the ball bumps 2. As a result, the LSI chip 1 is brought into contact with the ball electrodes 7. The following will explain the features of the above-explained semiconductor device having the ball grid array. The first feature lies in that the mount of the semiconductor device can be easily performed. Specifically, as shown in FIG. 2, a semiconductor device 100 is placed on a print circuit board 200, and heat is applied thereon, so that the mount of the semiconductor device can be completed. As shown in FIG. 3, the print circuit board 200 on which the semiconductor device 100 is mounted is moved via a reflow furnace 300. The ball

electrodes 7 of the semiconductor device 100 are temporarily melted when entering the reflow furnace 300. Then, when the electrodes 7 come out of the reflow furnace 300, the ball electrodes 7 are solidified again. At the time when the ball electrodes 7 are solidified again, they are combined with electrodes 8 of the print circuit board 200. (col. 1, lines 10-48)

Thus, *Hiruta* merely discloses that the ball bumps 2 are centered over the electrodes 6a. Nothing in *Hiruta* shows, teaches or suggests that the center of the solder bump is located off-set from a center of a substrate side pad as claimed in claim 7. Rather, *Hiruta* teaches away from the claimed invention since the ball electrode 7 are centered over the electrode 6b.

Since nothing in *Tanaka* or *Hiruta* show, teach or suggest a center of a solder bump located off-set from a center of the substrate-side pad as claimed in claim 7, it is respectfully requested that the Examiner withdraws the rejection to claim 7 under 35 U.S.C. §103.

Claim 8 depends from claim 7 and recites additional features. It is respectfully submitted that claim 8 would not have been obvious within the meaning of 35 U.S.C. §103 over *Tanaka* and *Hiruta* at least for the reasons as set forth above. Therefore, it is respectfully requested that the Examiner withdraws the rejection to claim 8 under 35 U.S.C. §103.

Thus it now appears that the application is in condition for reconsideration and allowance. Reconsideration and allowance at an early date are respectfully requested.

If for any reason Examiner feels that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed within the currently set shortened statutory period, applicants respectfully petition for an appropriate extension of time. The fees for such extension of time may be charged to our Deposit Account No. 02-4800.

In the event that any additional fees are due with this paper, please charge our Deposit Account No. 02-4800.

Respectfully submitted,

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